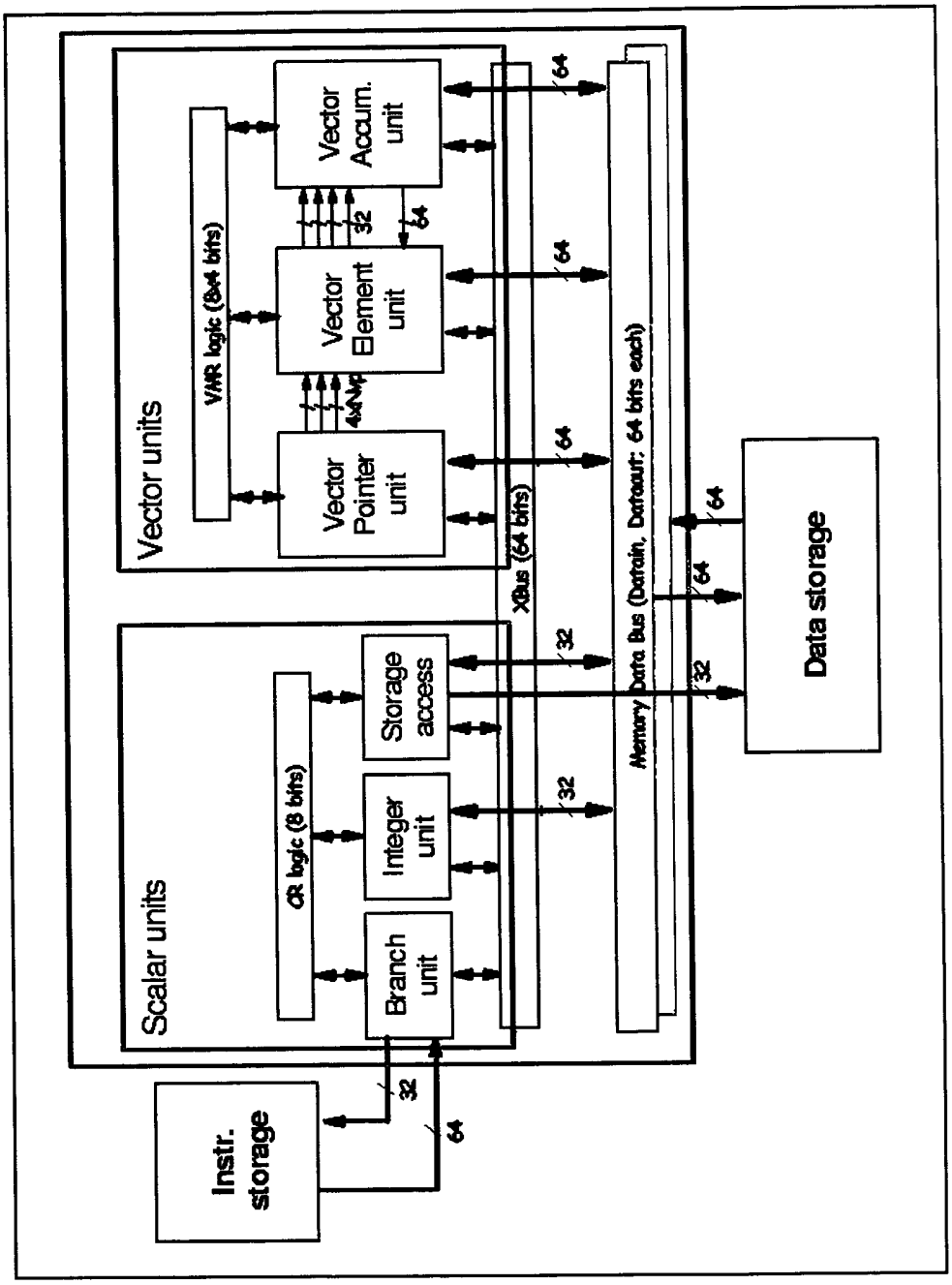
Vector units
VMR logic (8x4 bits)
Vector Accum. unit
Vector Element unit
Vector Pointer unit
Scalar units
CR logic (8 bits)
Storage access
Integer unit
Branch unit
XBus (64 bits)
Memory Data Bus (Datrain, Datraout: 64 bits each)
Data storage
Instr. storage
32
64

Fig. 1A

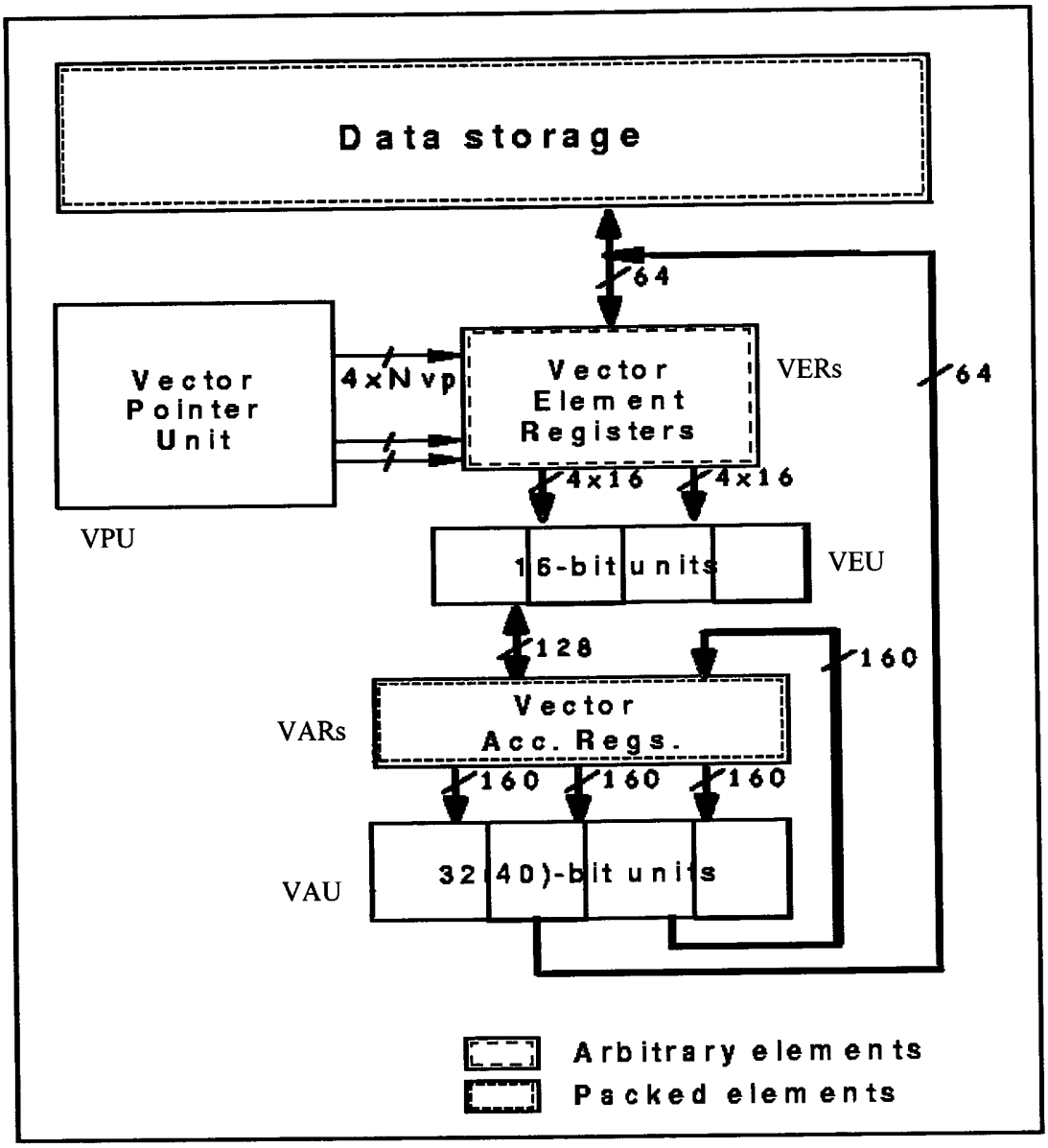
Data storage
64
Vector Pointer Unit
4xNvp
Vector Element Registers
VERs
64
4x16
4x16
VPU
16-bit units
VEU
128
160
VARs
Vector Acc. Regs.
160
160
160
VAU
32(40)-bit units
Arbitrary elements
Packed elements

Fig. 1B

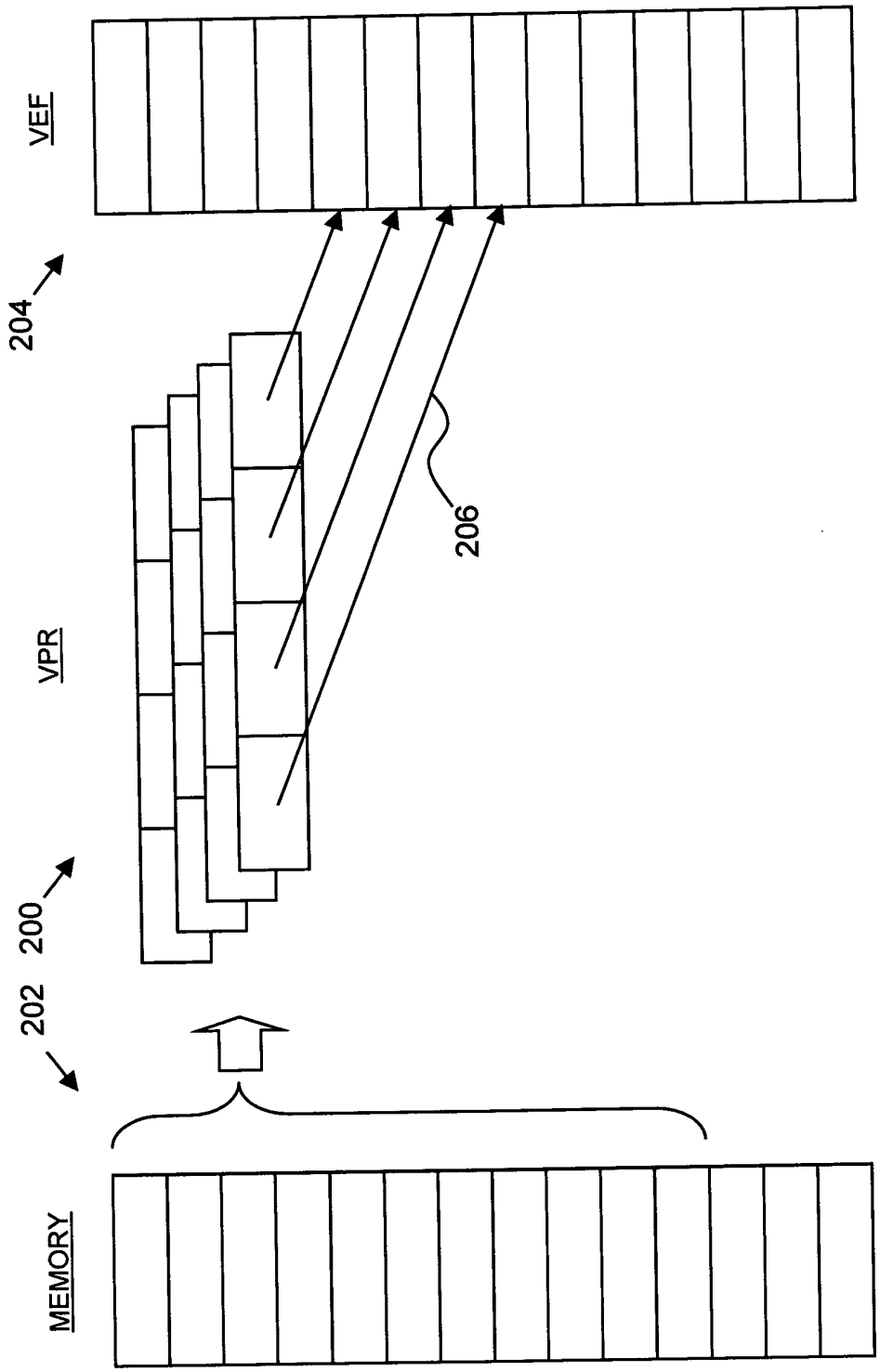

Fig. 2A

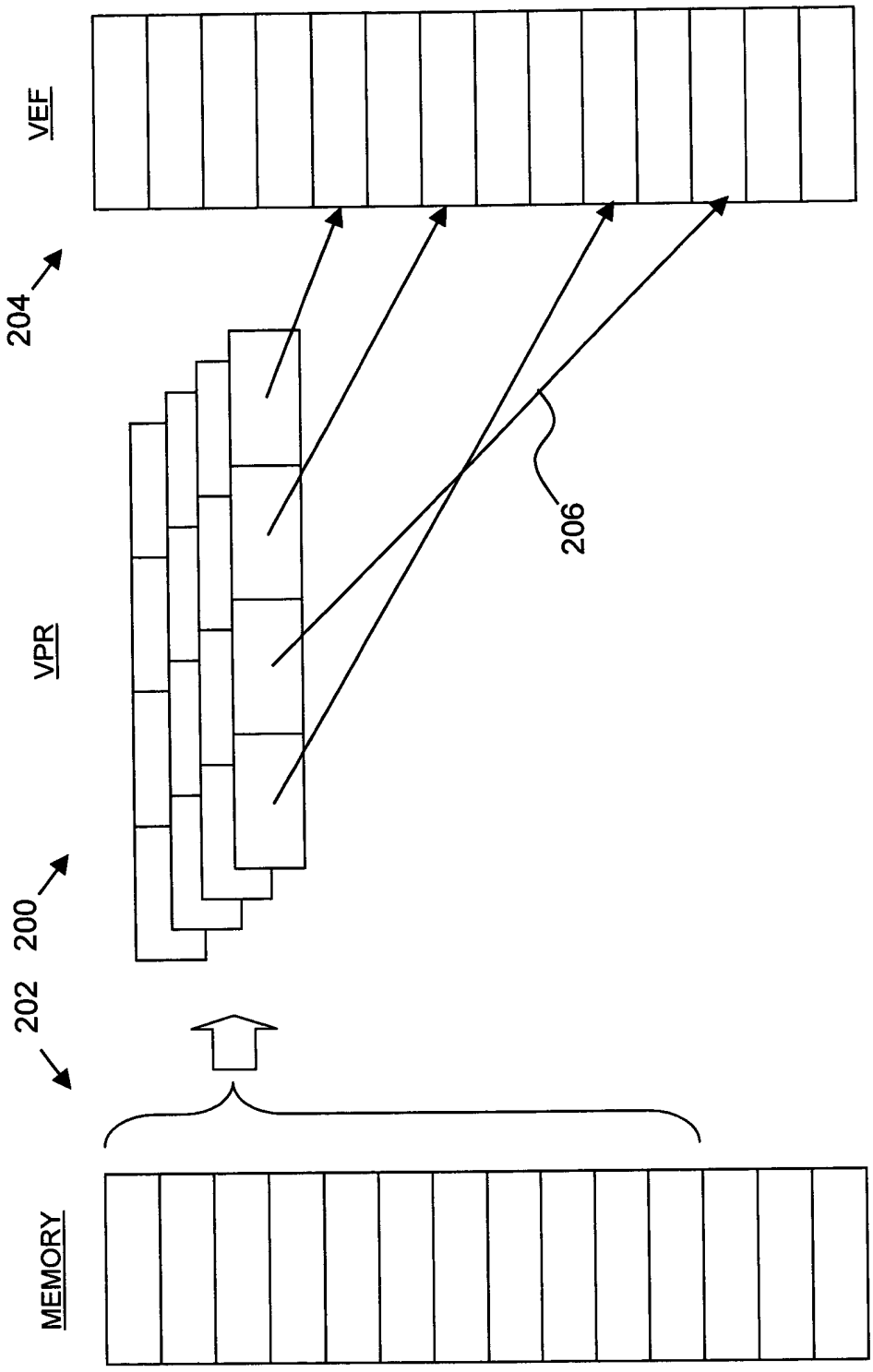

Fig. 2B

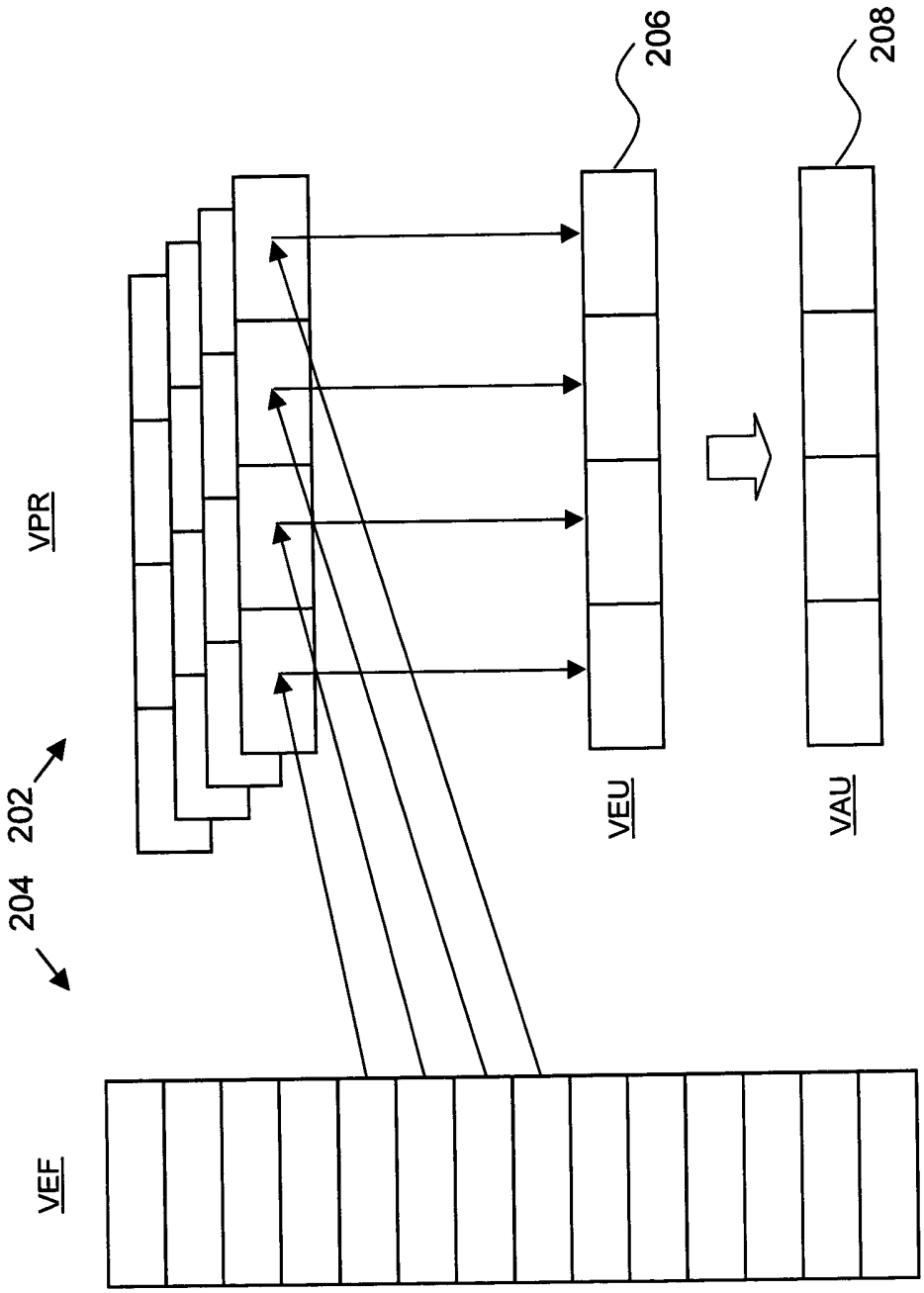

Fig. 2C

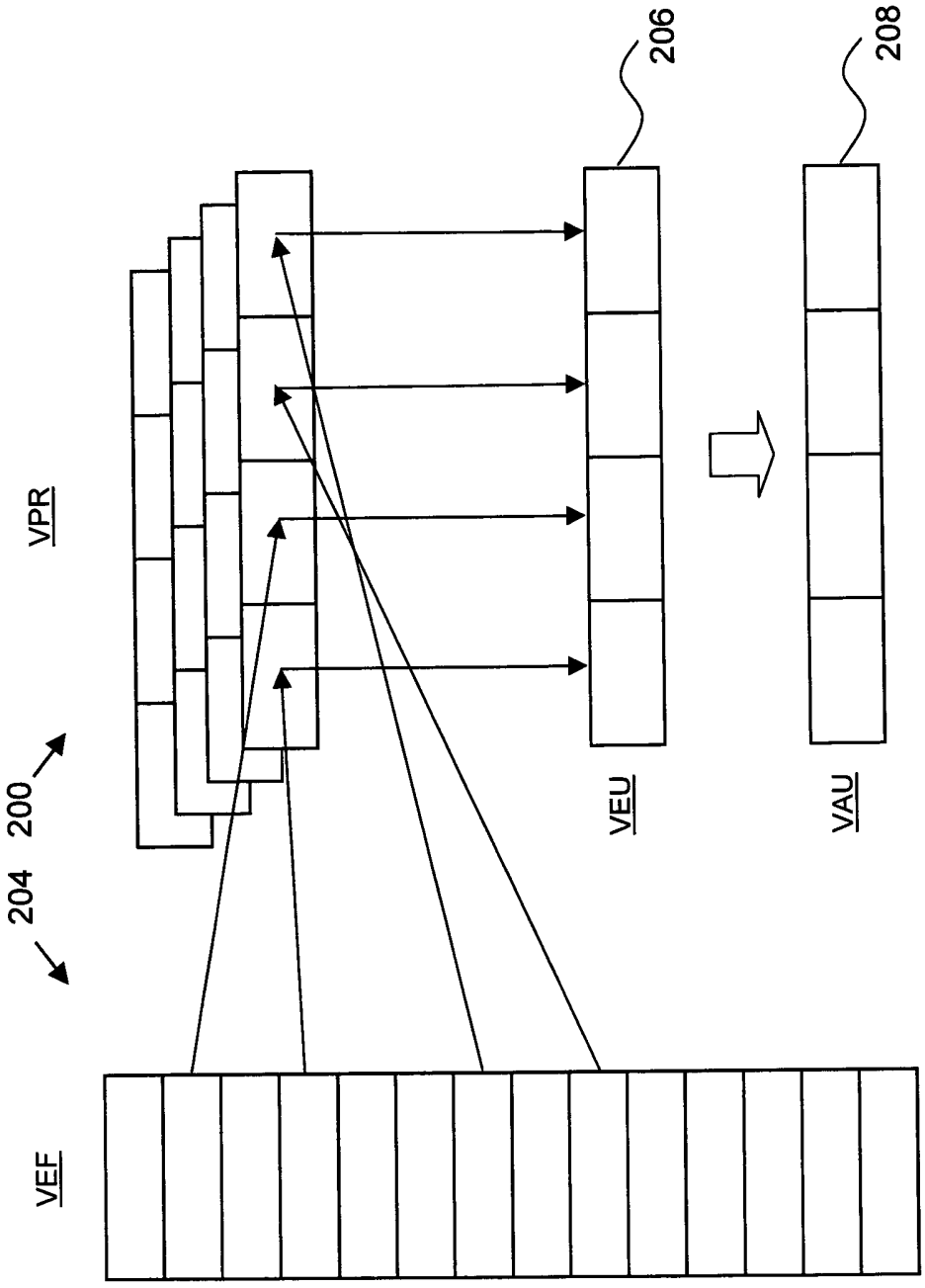

Fig. 2C

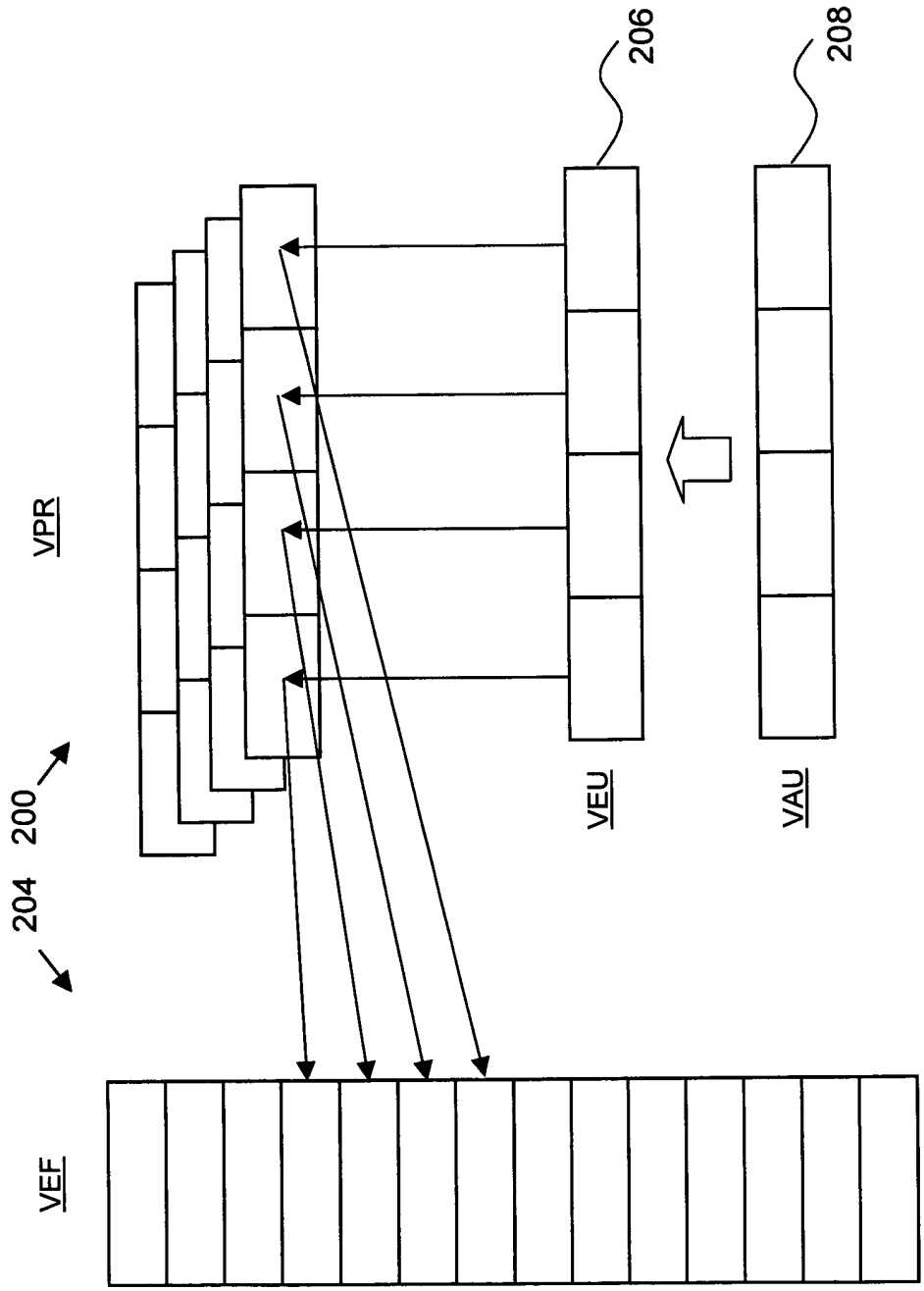

Fig. 2E

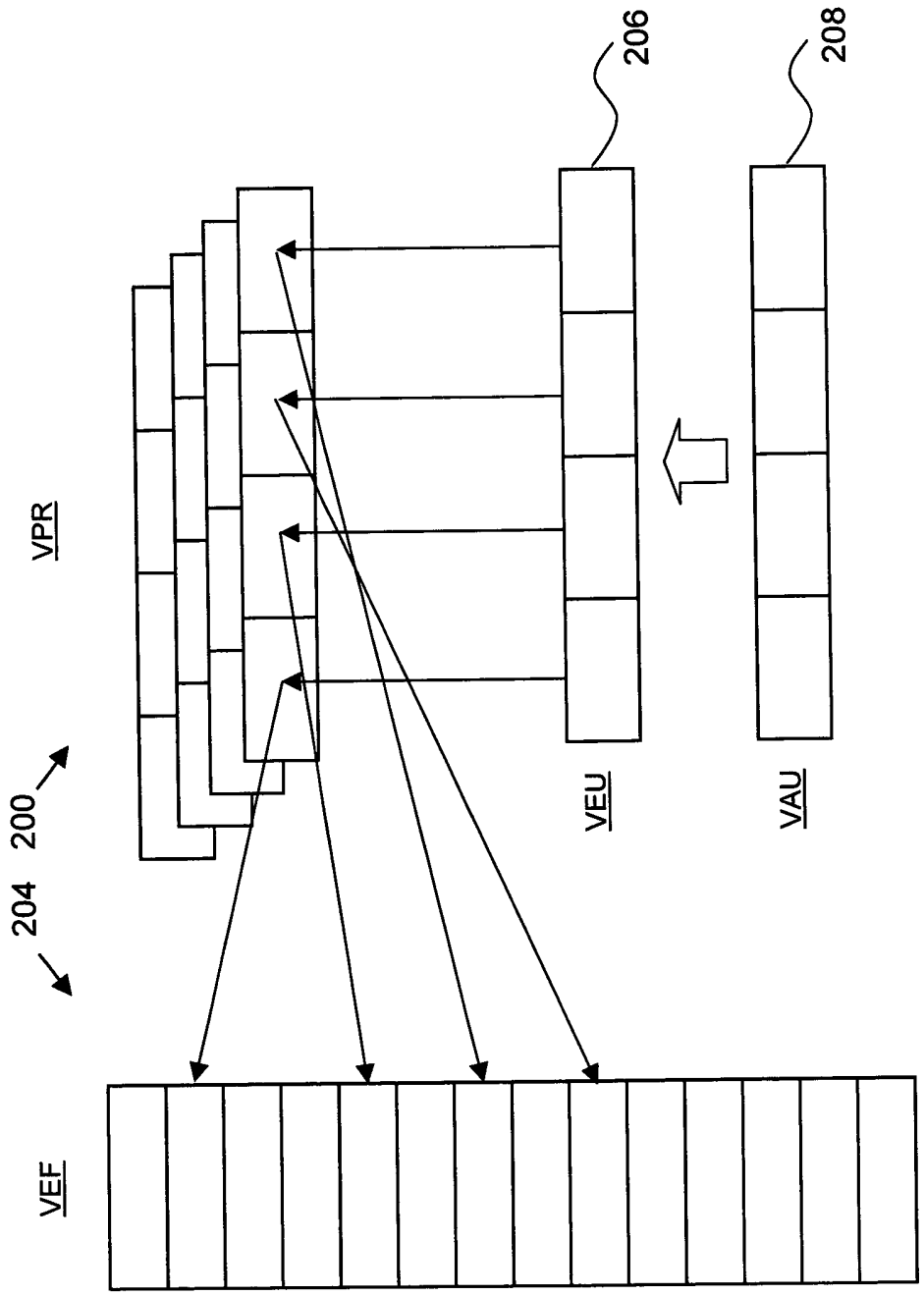

Fig. 2F

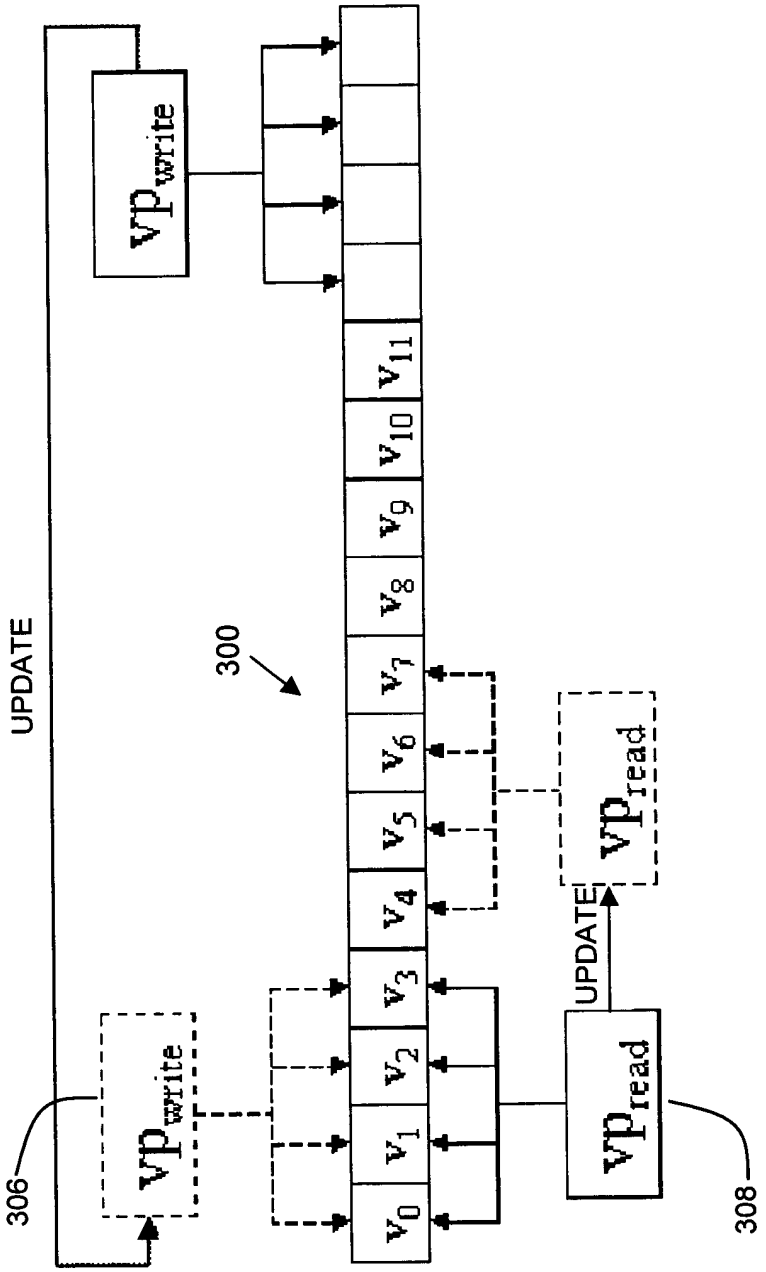
UPDATE
300
vp_{write}
v_{11}
v_{10}
v_9
v_8
v_7
v_6
v_5
v_4
v_3
v_2
v_1
v_0
vp_{read}
UPDATE
306
308

Fig. 3B

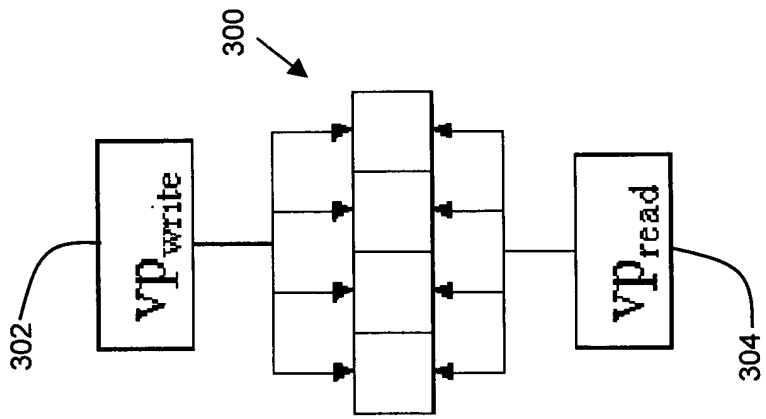
300
vp_{write}
vp_{read}
302
304

Fig. 3A

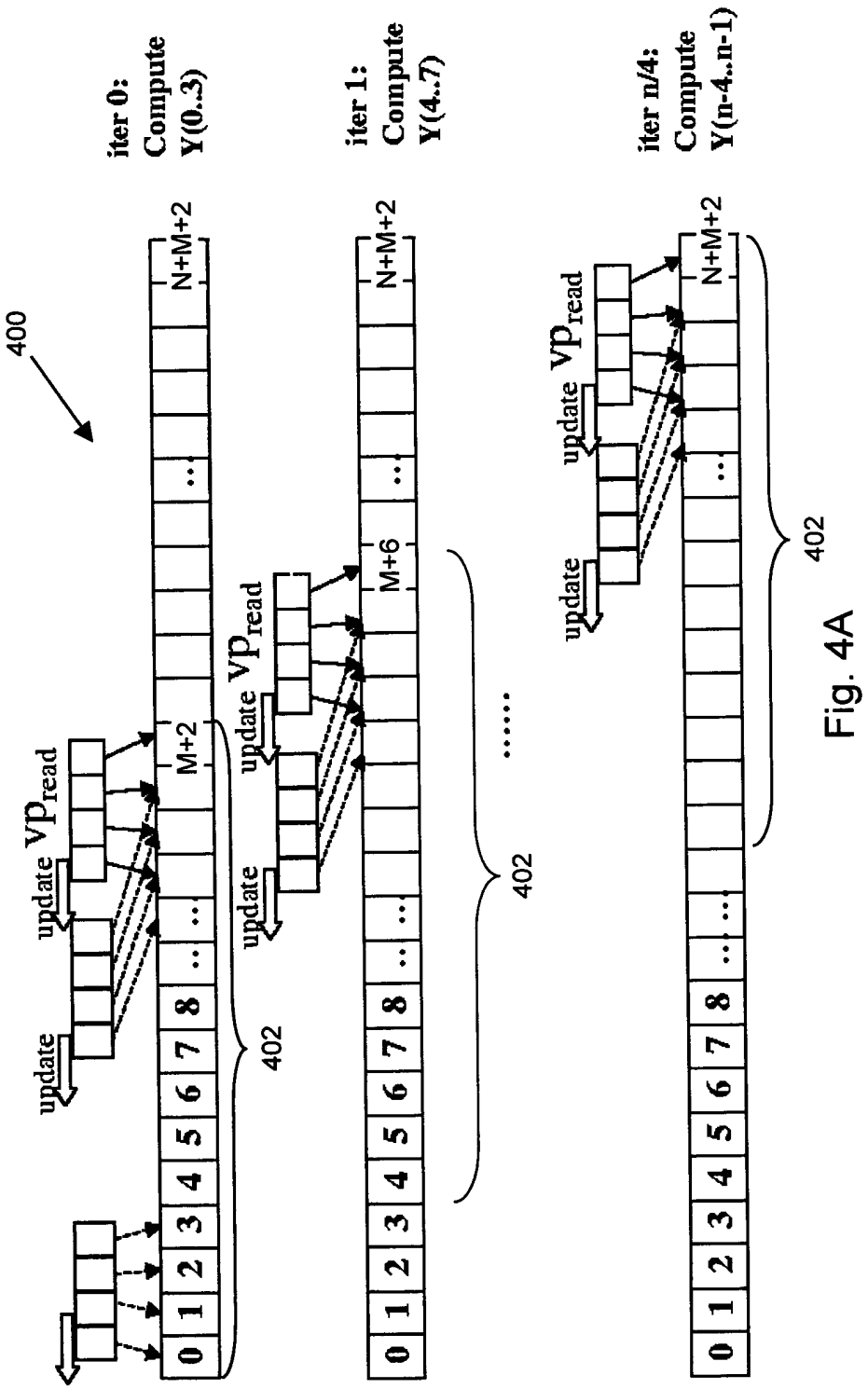
400
iter 0:
Compute
Y(0..3)
iter 1:
Compute
Y(4..7)
iter n/4:
Compute
Y(n-4..n-1)
update
vp_{read}
0 1 2 3 4 5 6 7 8 .. .. M+2 N+M+2
M+6
402
.....

Fig. 4A

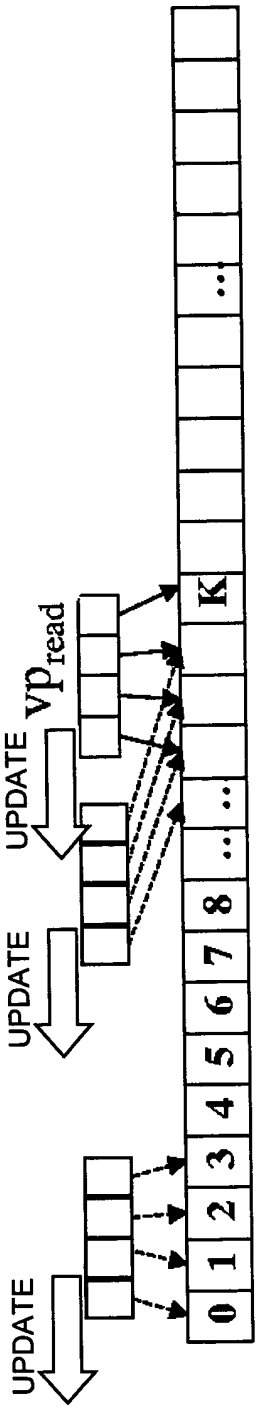

Fig. 4B

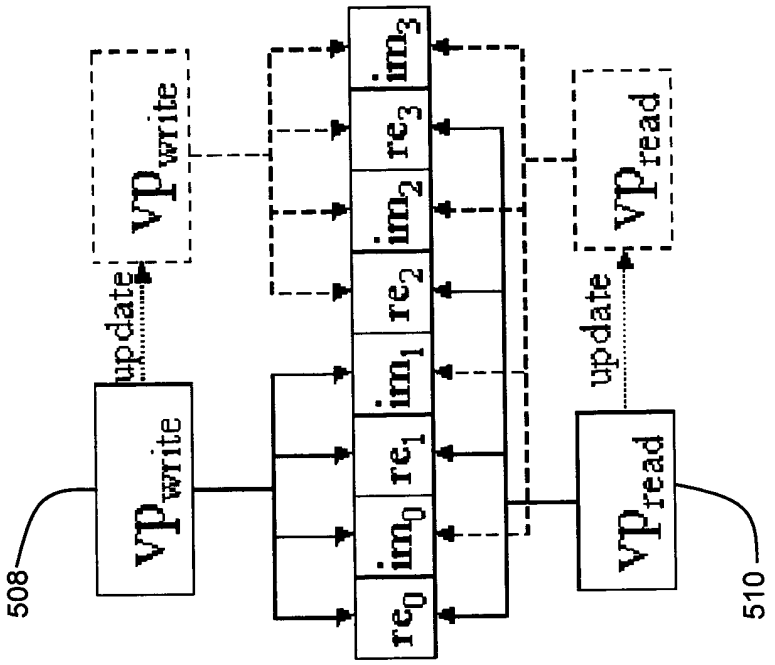
508
vp_{write}
update
vp_{write}
re_0 im_0 re_1 im_1 re_2 im_2 re_3 im_3
update
vp_{read}
vp_{read}
510

Fig. 5B

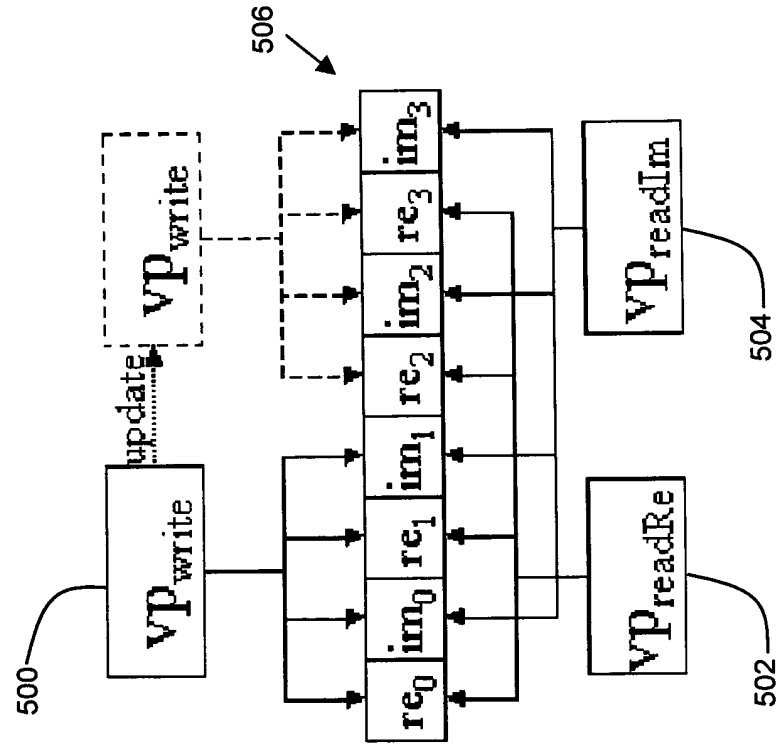
506
500
vp_{write}
update
vp_{write}
re_0 im_0 re_1 im_1 re_2 im_2 re_3 im_3
vp_{readIm}
504
vp_{readRe}
502

Fig. 5A

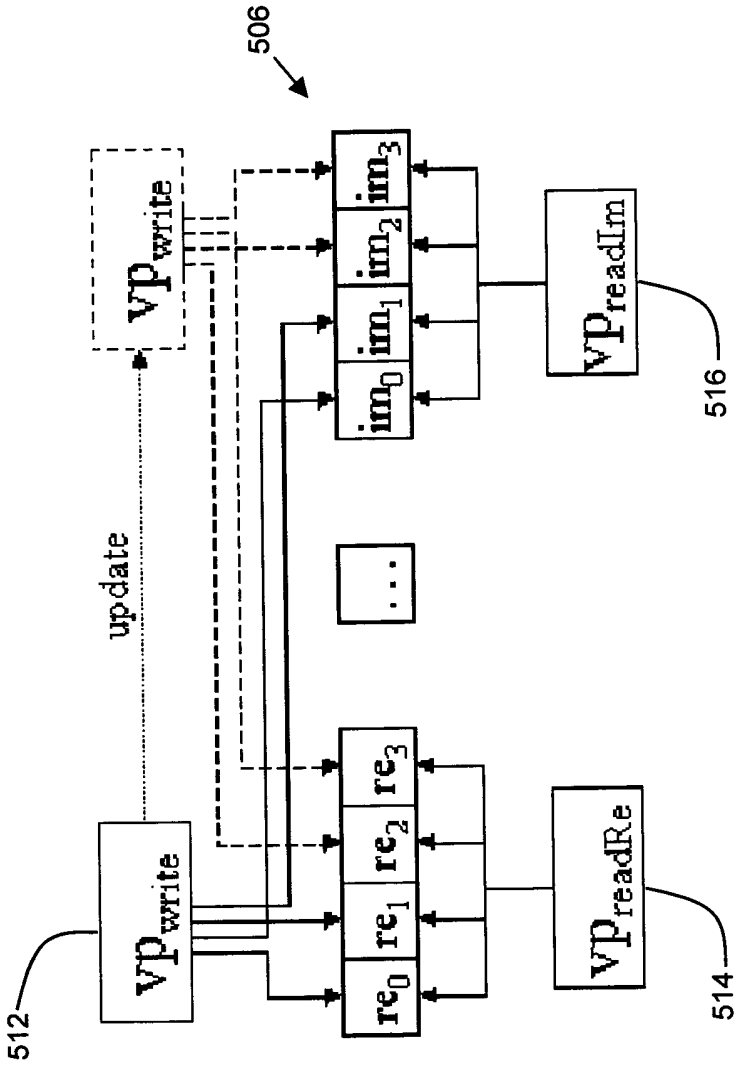
506
vp_{write}
im_3 im_2 im_1 im_0
vp_{readIm}
516
update
...
re_3 re_2 re_1 re_0
vp_{write}
vp_{readRe}
512
514

Fig. 5C

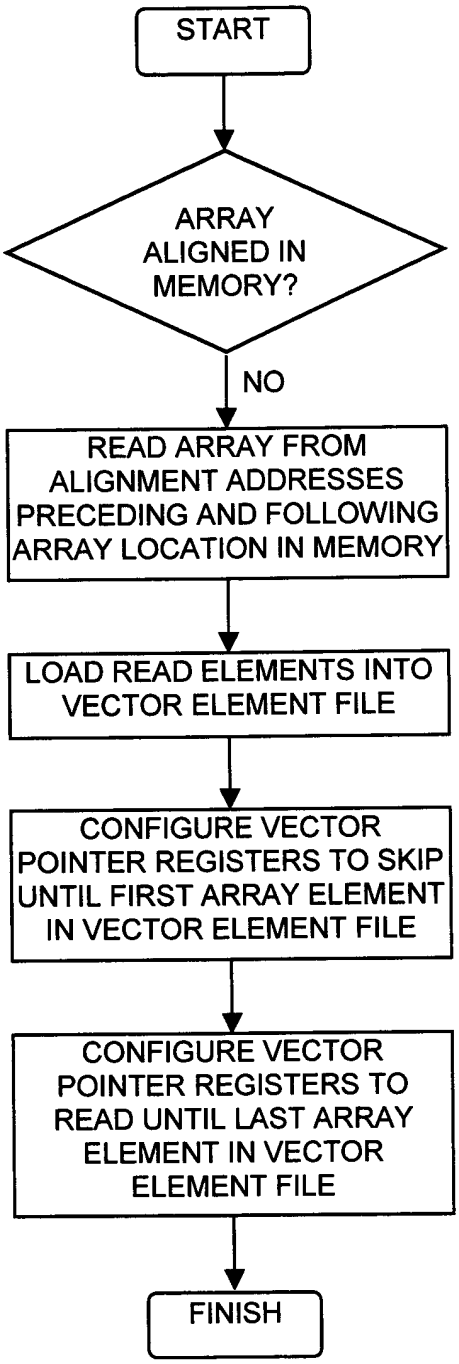
START
ARRAY ALIGNED IN MEMORY?
NO
READ ARRAY FROM ALIGNMENT ADDRESSES PRECEDING AND FOLLOWING ARRAY LOCATION IN MEMORY
LOAD READ ELEMENTS INTO VECTOR ELEMENT FILE
CONFIGURE VECTOR POINTER REGISTERS TO SKIP UNTIL FIRST ARRAY ELEMENT IN VECTOR ELEMENT FILE
CONFIGURE VECTOR POINTER REGISTERS TO READ UNTIL LAST ARRAY ELEMENT IN VECTOR ELEMENT FILE
FINISH

Fig. 6

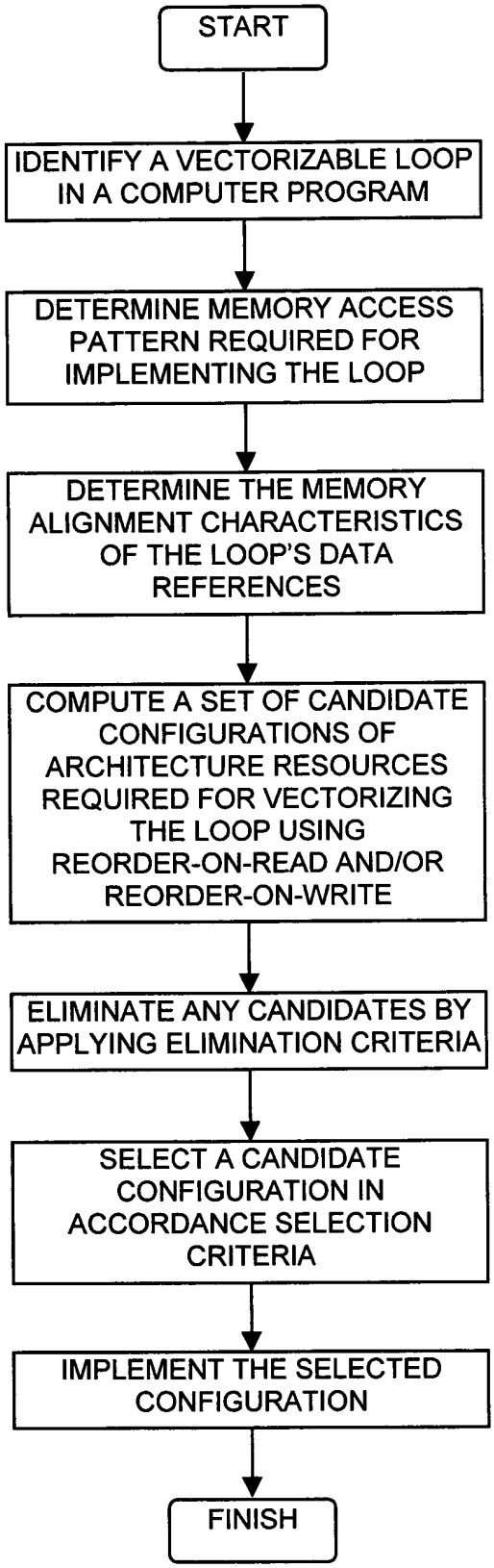
START
IDENTIFY A VECTORIZABLE LOOP IN A COMPUTER PROGRAM
DETERMINE MEMORY ACCESS PATTERN REQUIRED FOR IMPLEMENTING THE LOOP
DETERMINE THE MEMORY ALIGNMENT CHARACTERISTICS OF THE LOOP'S DATA REFERENCES
COMPUTE A SET OF CANDIDATE CONFIGURATIONS OF ARCHITECTURE RESOURCES REQUIRED FOR VECTORIZING THE LOOP USING REORDER-ON-READ AND/OR REORDER-ON-WRITE
ELIMINATE ANY CANDIDATES BY APPLYING ELIMINATION CRITERIA
SELECT A CANDIDATE CONFIGURATION IN ACCORDANCE SELECTION CRITERIA
IMPLEMENT THE SELECTED CONFIGURATION
FINISH

Fig. 7

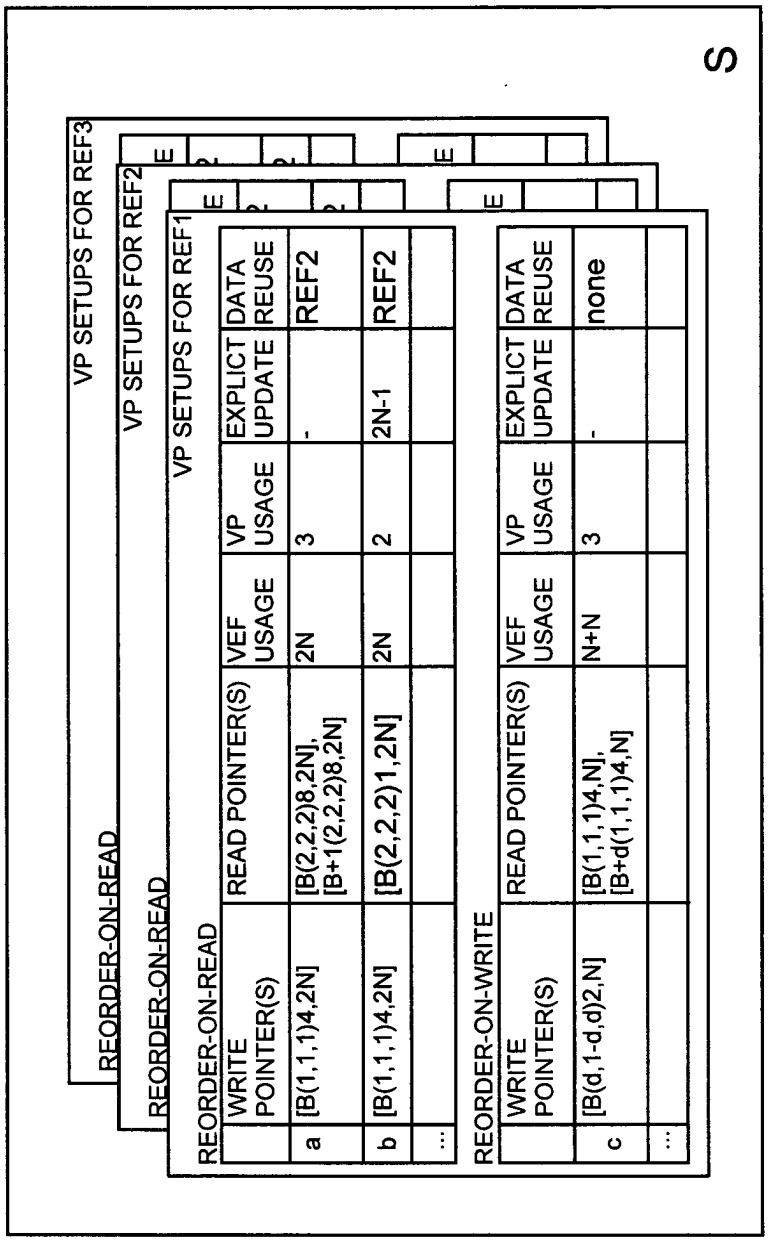
S
VP SETUPS FOR REF3
REORDER-ON-READ
VP SETUPS FOR REF2
REORDER-ON-READ
VP SETUPS FOR REF1
REORDER-ON-READ
WRITE POINTER(S)
READ POINTER(S)
VEF USAGE
VP USAGE
EXPLICT UPDATE
DATA REUSE
a
[B(1,1,1)4,2N]
[B(2,2,2)8,2N], [B+1(2,2,2)8,2N]
2N
3
-
REF2
b
[B(1,1,1)4,2N]
[B(2,2,2)1,2N]
2N
2
2N-1
REF2
...
REORDER-ON-WRITE
WRITE POINTER(S)
READ POINTER(S)
VEF USAGE
VP USAGE
EXPLICT UPDATE
DATA REUSE
c
[B(d,1-d,d)2,N]
[B(1,1,1)4,N], [B+d(1,1,1)4,N]
N+N
3
-
none
...

Fig. 8

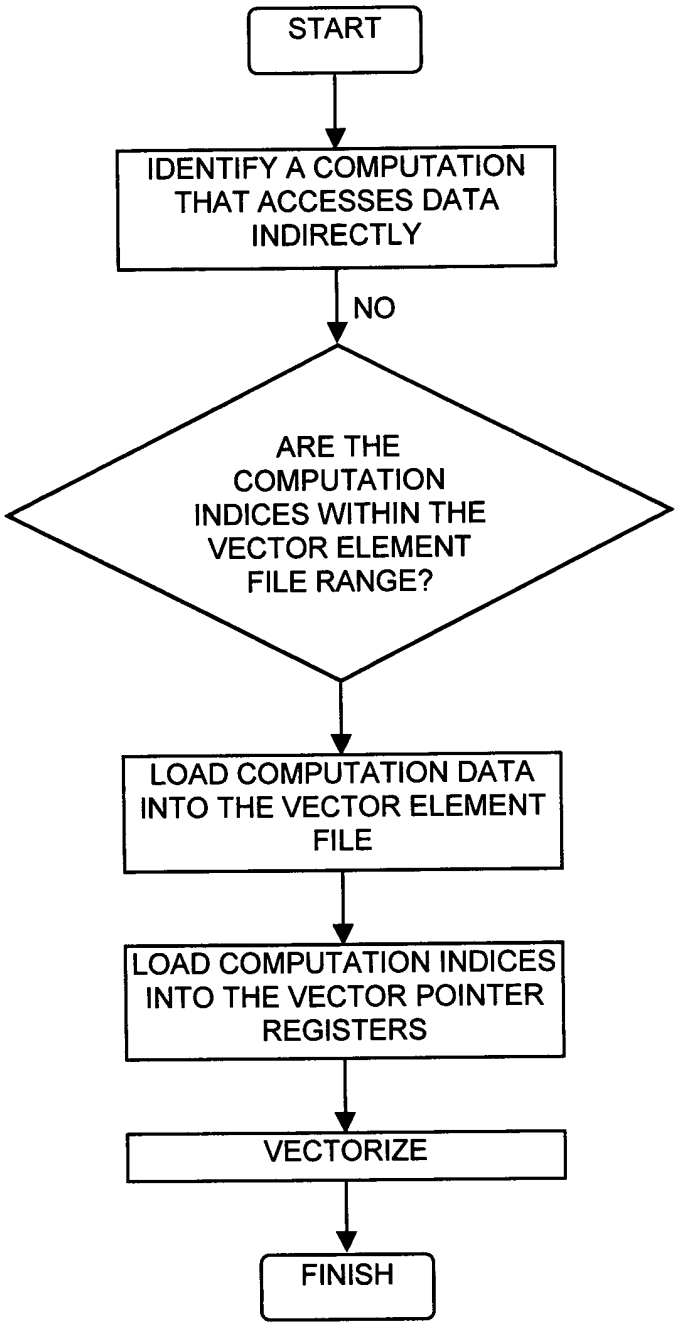
START
IDENTIFY A COMPUTATION THAT ACCESSES DATA INDIRECTLY
NO
ARE THE COMPUTATION INDICES WITHIN THE VECTOR ELEMENT FILE RANGE?
LOAD COMPUTATION DATA INTO THE VECTOR ELEMENT FILE
LOAD COMPUTATION INDICES INTO THE VECTOR POINTER REGISTERS
VECTORIZE
FINISH

Fig. 9